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UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))		Attorney Docket No.	MI22-898
		First Inventor or Application Identifier	Pai-Hung Pan
		Title	Semiconductor Processing Methods of...
		Express Mail Label No.	EL054827024US

APPLICATION ELEMENTS See MPEP chapter 600 concerning utility patent application contents.	ADDRESS TO: Assistant Commissioner for Patents Box Patent Application Washington, DC 20231
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1. <input checked="" type="checkbox"/> * Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original, and a duplicate for fee processing) 2. <input checked="" type="checkbox"/> Specification [Total Pages 28] + cover sheet - Descriptive title of the invention - Cross References to Related Applications - Statement Regarding Fed sponsored R & D - Reference to Microfiche Appendix - Background of the Invention - Brief Summary of the Invention - Brief Description of the Drawings (if filed) - Detailed Description - Claim(s) - Abstract of the Disclosure 3. <input checked="" type="checkbox"/> Drawing(s) (35 U.S.C. 113) [Total Sheets 4] 4. Oath or Declaration [Total Pages] a. <input type="checkbox"/> Newly executed (original or copy) b. <input checked="" type="checkbox"/> Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 17 completed) (Note Box 5 below) i. <input type="checkbox"/> DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b). 5. <input checked="" type="checkbox"/> Incorporation By Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein	6. <input type="checkbox"/> Microfiche Computer Program (Appendix) 7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary) a. <input type="checkbox"/> Computer Readable Copy b. <input type="checkbox"/> Paper Copy (identical to computer copy) c. <input type="checkbox"/> Statement verifying identity of above copies
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ACCOMPANYING APPLICATION PARTS	
8. <input type="checkbox"/> Assignment Papers (cover sheet & document(s)) 9. <input checked="" type="checkbox"/> 37 C.F.R. § 3.73(b) Statement (when there is an assignee) <input type="checkbox"/> Power of Attorney 10. <input type="checkbox"/> English Translation Document (if applicable) 11. <input checked="" type="checkbox"/> Information Disclosure Statement (IDS)/PTO-1449 <input type="checkbox"/> Copies of IDS Citations 12. <input checked="" type="checkbox"/> Preliminary Amendment 13. <input checked="" type="checkbox"/> Return Receipt Postcard (MPEP 503) (Should be specifically itemized) * Small Entry 14. <input type="checkbox"/> Statement(s) <input type="checkbox"/> Statement filed in prior application (PTO/SB/09-12) <input type="checkbox"/> Status still proper and desired 15. <input type="checkbox"/> Certified Copy of Priority Document(s) (if foreign priority is claimed) 16. <input checked="" type="checkbox"/> Other: Check, Substitute Drawing Request	* A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon

17. If a CONTINUING APPLICATION check appropriate box, and supply the requisite information below and in a preliminary amendment: <input checked="" type="checkbox"/> Continuation <input type="checkbox"/> Divisional <input type="checkbox"/> Continuation-in-part (CIP) of prior application No: 08 / 710,353 Prior application information: Examiner B. Mee Group / Art Unit: 1107	
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18. CORRESPONDENCE ADDRESS <input type="checkbox"/> Customer Number or Bar Code Label (Insert Customer No. or Attach bar code label here) or <input checked="" type="checkbox"/> Correspondence address below					
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FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1.
These are the fees effective October 1, 1997.
Small Entity payments must be supported by a small entity statement,
otherwise large entity fees must be paid. See Forms PTO/SB/09-12.

TOTAL AMOUNT OF PAYMENT (\$ 872.00

Complete if Known

Application Number PRIORITY 08/710,353
Filing Date Filed Herewith
First Named Inventor Pai-Hung Pan
Examiner Name PRIORITY B. Mee
Group / Art Unit PRIORITY 1107
Attorney Docket No. MI22-898

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number 23-0925
Deposit Account Name Wells, St. John, et al.

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17 ☐ Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

2. ☒ Payment Enclosed:

☒ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
101 790	201 395	Utility filing fee	790
106 330	206 165	Design filing fee	
107 540	207 270	Plant filing fee	
108 790	208 395	Reissue filing fee	
114 150	214 75	Provisional filing fee	
SUBTOTAL (1)			790

2. EXTRA CLAIM FEES

Total Claims 12 -20** = 0 X Fee from below 22 = 0
Independent Claims 4 - 3** = 1 X 82 = 82
Multiple Dependent ☐ = ☐

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
103 22	203 11	Claims in excess of 20	
102 82	202 41	Independent claims in excess of 3	
104 270	204 135	Multiple dependent claim, if not paid	
109 82	209 41	** Reissue independent claims over original patent	
110 22	210 11	** Reissue claims in excess of 20 and over original patent	
SUBTOTAL (2)			82

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
105 130	205 65	Surcharge - late filing fee or oath	
127 50	227 25	Surcharge - late provisional filing fee or cover sheet.	
139 130	139 130	Non-English specification	
147 2,520	147 2,520	For filing a request for reexamination	
112 920*	112 920*	Requesting publication of SIR prior to Examiner action	
113 1,840*	113 1,840*	Requesting publication of SIR after Examiner action	
115 110	215 55	Extension for reply within first month	
116 400	216 200	Extension for reply within second month	
117 950	217 475	Extension for reply within third month	
118 1,510	218 755	Extension for reply within fourth month	
128 2,060	228 1,030	Extension for reply within fifth month	
119 310	219 155	Notice of Appeal	
120 310	220 155	Filing a brief in support of an appeal	
121 270	221 135	Request for oral hearing	
138 1,510	138 1,510	Petition to institute a public use proceeding	
140 110	240 55	Petition to revive - unavoidable	
141 1,320	241 660	Petition to revive - unintentional	
142 1,320	242 660	Utility issue fee (or reissue)	
143 450	243 225	Design issue fee	
144 670	244 335	Plant issue fee	
122 130	122 130	Petitions to the Commissioner	
123 50	123 50	Petitions related to provisional applications	
126 240	126 240	Submission of Information Disclosure Stmt	
581 40	581 40	Recording each patent assignment per property (times number of properties)	
146 790	246 395	Filing a submission after final rejection (37 CFR 1.129(a))	
149 790	249 395	For each additional invention to be examined (37 CFR 1.129(b))	
Other fee (specify) _____			
Other fee (specify) _____			
* Reduced by Basic Filing Fee Paid			
SUBTOTAL (3)			0

SUBMITTED BY

Typed or Printed Name LANCE R. SADLER

Signature

Date

4/13/98

Complete (if applicable)

Reg. Number 38,605

Deposit Account User ID

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EL054827024

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Semiconductor Processing Methods Of Forming A
Conductive Gate And Line

* * * * *

INVENTOR

Pai-Hung Pan

ATTORNEY'S DOCKET NO. MI22-488

EL054827 024

EM

TECHNICAL FIELD

This invention relates to semiconductor processing methods of forming a conductive gate line.

BACKGROUND OF THE INVENTION

Metal Oxide Semiconductor (MOS) devices find use in integrated circuit memory devices such as static random access memory (SRAM) and dynamic random access memory (DRAM) devices. Such devices inevitably include conductive lines connecting one or more of the devices together. One type of conductive line is a gate or word line. Word lines connect the gates of one or more MOS devices together so that when the word line is turned on, data in the form of stored charges can be accessed.

It is desirable that a word line be highly conductive. A great deal of effort has gone into engineering more conductive word lines. Words lines are typically formed over a dielectric surface. The conventional word line includes at least one layer of conductive material which is layered onto the dielectric surface and then etched, typically anisotropically, to form a patterned word line, also referred to herein as a gate, gate line or gate stack. After anisotropically etching the gate or gate line, it is desirable to conduct a reoxidation step which helps to repair damage to the dielectric surface resulting from the anisotropic etch. Additionally, the reoxidation step oxidizes a portion of the gate or gate stack immediately adjacent the dielectric surface to

round the lower portion of the conductive material, effectively creating a so-called "smiling gate" structure in which tiny bird's beak structures are formed at the bottom corners of the gate stack. Such smiling gate structure reduces hot electron degradation, as recognized by those of skill in the art.

During such reoxidation steps, it has been observed that the conductivity of the gate has been impaired due to the undesirable oxidation of the conductive materials forming the gate. For example, one type of conductive gate includes a conductive polysilicon layer atop the dielectric surface and a conductive layer of WSi_x atop the polysilicon layer. A more conductive prior art word line is formed from a conductive layer of polysilicon, a conductive layer of metallic material, and an intervening conductive metallic barrier layer between the polysilicon and metallic material which prevents formation of silicide during subsequent processing. Unfortunately, during the reoxidation step, the conductive materials of the line experience appreciable oxidation which has led to higher resistances (lower conductivities). Additionally, such oxidation has led to degradation of the interface between the materials which, in turn, can cause the materials to peel away from one another and create a yield loss.

This invention grew out of the need to provide a conductive line and to reduce undesirable oxidation effects on the conductive line due to oxidation processing steps such as a source/drain oxidation.

1 BRIEF DESCRIPTION OF THE DRAWINGS

2 Preferred embodiments of the invention are described below with
3 reference to the following accompanying drawings.

4 Fig. 1 is a diagrammatic representation of a fragment of a
5 substrate processed in accordance with the invention.

6 Fig. 2 is a view of the Fig. 1 substrate fragment at a processing
7 step subsequent to that shown by Fig. 1.

8 Fig. 3 is a view of the Fig. 1 substrate fragment at a processing
9 step subsequent to that shown by Fig. 2.

10 Fig. 4 is a view of the Fig. 1 substrate fragment at a processing
11 step subsequent to that shown by Fig. 3.

12 Fig. 5 is a view of the Fig. 1 substrate fragment at a processing
13 step subsequent to that shown by Fig. 4.

14 Fig. 6 is a view of the Fig. 1 substrate fragment at a processing
15 step subsequent to that shown by Fig. 2 in accordance with an alternate
16 preferred embodiment of the invention.

17 Fig. 7 is a view of the Fig. 1 substrate fragment at a processing
18 step subsequent to that shown by Fig. 6.

19 Fig. 8 is an enlarged view of a portion of the wafer fragment of
20 Fig. 3 undergoing a smiling gate oxidation.

005544-011399

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

In accordance with one aspect of the invention, a semiconductor processing method of forming a conductive transistor gate over a substrate comprises the steps of:

forming a conductive gate over a gate dielectric layer on a substrate, the gate having sidewalls and an interface with the gate dielectric layer;

forming nitride containing spacers over the gate sidewalls; and
after forming the spacers, exposing the substrate to oxidizing conditions effective to oxidize at least a portion of the gate interface with the gate dielectric layer.

In accordance with another aspect of the invention, a semiconductor processing method of forming a conductive gate comprises the steps of:

forming a patterned gate atop a substrate dielectric surface, at least a portion of the gate being conductive;

covering the gate with oxidation resistant material; and

exposing the substrate to oxidation conditions effective to oxidize at least a portion of the gate laterally adjacent the oxidation barriers

1 In accordance with yet another aspect of the invention, a
2 semiconductor processing method of forming a conductive transistor gate
3 over a substrate comprises the steps of:

4 forming a conductive gate over a gate dielectric layer on a
5 substrate, the gate having sidewalls;

6 forming non-oxide spacers over the sidewalls; and

7 after forming the spacers, exposing the substrate to oxidizing
8 conditions effective to oxidize at least a portion of the gate and a
9 portion of the substrate beneath the gate.

10 More specifically and with reference to Fig. 1, a semiconductor
11 wafer fragment in process is indicated generally by reference
12 numeral 10. Such is comprised of a bulk substrate 12, preferably
13 composed of monocrystalline silicon, and an overlying dielectric layer 14
14 in the form of a suitable gate oxide. Dielectric layer 14 defines a
15 substrate dielectric surface atop which a patterned composite gate or
16 gate stack 16 is formed, preferably by an anisotropic reactive ion etch.
17 Gate stack 16 defines a field effect transistor gate line at least a
18 portion of which is conductive. Gate stack 16 includes a pair of
19 sidewalls 18, 20 and an interface 22 with gate dielectric layer 14. Gate
20 stack 16 is a multi-layered structural composite which includes a
21 plurality of layers. A first conductive layer 24 is preferably formed
22 from polysilicon and includes a portion which defines interface 22. A
23 metal layer 26 overlies layer 24 and is formed from a suitable metal
24 such as tungsten (W), molybdenum (Mo) and the like. An electrically

conductive reaction barrier layer 28 is preferably formed from a suitable material such as TiN, WN, and the like and is interposed between or intermediate layers 24 and 26. Layer 28 in the preferred embodiment prevents the formation of a silicide during subsequent processing steps. A cap 30 is formed atop overlying metal layer 26 from a suitable oxidation resistant material such as oxide/nitride, nitride, oxide/nitride/oxide, oxynitride, Si-rich nitride and the like, for protecting or shielding gate stack 16 during a subsequent oxidation step described in detail below. Accordingly, cap 30 is a nitride containing material which effectively protects or shields the top of the gate line as will become apparent below.

Referring to Figs. 2 and 3, first oxidation barriers are formed on gate stack 16 which cover at least the conductive portion of the gate stack. First oxidation barriers can be formed from nitride containing material and/or suitable non-oxide materials. More specifically, first oxidation barrier material 32, such as Si_3N_4 or SiN_xO_y , is deposited over gate stack 16 (Fig. 2) to a thickness ranging from between 50 to 500 Angstroms. Such can be deposited utilizing conventional techniques at deposition temperatures between 300°C - 900°C . A subsequent first anisotropic etch (Fig. 3) is conducted to a degree sufficient to leave first oxidation barriers 34, 36 on or proximate gate stack 16. Preferably, such etch is a reactive ion etch which is selective to oxide. Oxidation barriers 34, 36 preferably shield at least a portion of gate line sidewalls 18, 20 during subsequent processing, which includes a

reoxidation step described below. For purposes of the ongoing discussion, first oxidation barrier material 32 comprises a first insulative or insulating material which is anisotropically etched to form electrically insulative or insulating spacers 34, 36 over gate line sidewalls 18, 20, respectively.

According to one preferred aspect of the invention, and after spacers or barriers 34, 36 are formed, the substrate is exposed to oxidizing conditions which are effective to reoxidize the substrate to repair damage to layer 14 resulting from the first etch, as well as to oxidize at least a portion of the gate or gate line interface 22 with dielectric layer 14. During such exposure cap 30 together with barriers 34, 36 effectively encapsulate or cover the gate thereby preferably shielding the gate top and desired portions of the gate sidewalls from the effects of oxidation. Suitable oxidizing conditions have been found to be those which are conducted at ambient temperatures in a range from between about 800°C to 1050°C for time periods which would be sufficient to grow an oxide layer over a separate semiconductor substrate to a thickness of around 80 Angstroms. Other oxidizing conditions are possible. Such oxidation is best seen in Fig. 8 which is an enlarged partial view of gate or gate stack 16. There, bottom corner portions of polysilicon layer 24 laterally adjacent spacers 34, 36 are suitably oxidized and thereby rounded to form a smiling gate. More specifically, oxidants indicated by the small arrows entering into and through gate dielectric layer 14 channel along and through dielectric

layer 14. That is, layer 14 provides a channeling layer through which oxidants can travel to reach the gate or gate stack. Preferably during the smiling gate oxidation, the portion of gate stack 16 which is oxidized is disposed laterally adjacent and inwardly of barriers or spacers 34, 36 and forms a "bird's beak" structure immediately adjacent each respective spacer. By controlling the oxidation temperature and time as mentioned above, the oxidation will occur at preferred gate edge regions and will not appreciably propagate upwardly towards layers 26, 28.

The smiling gate oxidation step may, however, be conducted at processing points other than immediately following the formation of spacers 34, 36. Such is described by way of example immediately below.

Referring to Fig. 4, another preferred aspect of the invention is set forth in which the smiling gate oxidation step is conducted after a second barrier material 38 is deposited over substrate 12, and more specifically, deposited over barriers or spacers 34, 36 which are defined by first barrier material 32. Preferably, the second barrier material is a nitride containing and/or non-oxide material deposited to a thickness of 500 Angstroms. For purposes of the ongoing discussion, second barrier material 38 is a second oxidation resistant layer or an electrically insulating or insulative material.

Referring to Fig. 5, a second anisotropic etch, preferably a reactive ion etch of second barrier material 38 is conducted to a degree

1 sufficient to leave second oxidation barriers 40, 42 over or proximate
2 first oxidation barriers 34, 36 respectively. At this point, the smiling
3 gate oxidation can take place to form the smiling gate as described
4 above with reference to Fig. 8. The step of exposing the substrate to
5 the oxidation conditions sufficient to form the smiling gate as described
6 above, can take place prior to depositing second barrier material 38 and
7 after the first anisotropic etch. Such step would take place in
8 conjunction with gate stack 16 as shown in Fig. 3.

9 Referring to Fig. 6, another preferred aspect of the invention is
10 set forth in which the smiling gate oxidation step takes place after
11 contemporaneous formation of the first and second oxidation barriers.
12 Specifically, first and second barrier materials or layers 32, 38 are
13 deposited over gate stack 16 as shown without anisotropic etch of
14 layer 32 prior to provision of layer 38. Preferably, the respective
15 thickness of such layers are 100 Angstroms (layer 32) and 500
16 Angstroms (layer 38).

17 Referring to Fig. 7, an anisotropic etch, preferably a reactive ion
18 etch of first and second barrier materials 32, 38 is conducted to a
19 degree sufficient to leave oxidation barriers 44, 46 on or over gate
20 stack 16. When oxidation barriers are formed according to this aspect
21 of the present method, the resulting barriers or spacers have a
22 construction which is somewhat different from that shown in Fig. 5.
23 More specifically, first or inner spacers 48, 50 include a bottom portion
24 which abuts dielectric layer 14 and extends laterally away from gate

stack 16 forming an L-shape (spacer 50) or a reverse L-shape (spacer 48).

After gate line sidewalls 18, 20 have been suitably electrically insulated, substrate 12 is exposed to oxidizing conditions which are effective to oxidize at least a portion of gate line interface 22 as described above, thereby forming the desired smiling gate construction. The anisotropic etch which is conducted with reference to Figs. 6 and 7, is a common step anisotropic etch which contemporaneously forms the desired spacers or barriers described above.

The preferred methods of forming the desired smiling gate structure include, first shielding the gate or gate line sidewalls or conductive portions thereof with a suitable shielding material, and then conducting a reoxidation step, such as a source/drain reoxidation step, which utilizes dielectric layer 14 as a suitable channeling layer or medium along and through which oxidants travel to reach first conductive layer 24 so as to oxidize a portion thereof and a portion of the substrate therebeneath. According to a preferred aspect the shielding step includes, in a separate step, forming cap 30 over the gate top to protect the gate top during oxidation exposure. The oxidation barriers, whether barriers 34, 36 (Fig. 3), barrier pairs 34/40, 36/42 (Fig. 5), or barrier pairs 44/48, 46/50 (Fig. 7), serve to protect, along with oxidation resistant cap 30, the transistor gate or gate line stack from being undesirably affected by the reoxidation step which creates the smiling gate construction. This is because during such reoxidation step,

the materials utilized to form composite gate stack 16 are effectively encapsulated or covered with oxidation barriers and sealed. Such serves to protect against undesirable chemical reactions with the oxidants. Such chemical reactions, if allowed to take place, would undesirably erode or oxidize the gate stack materials.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A semiconductor processing method of forming a conductive transistor gate over a substrate comprising the steps of:

forming a conductive gate over a gate dielectric layer on a substrate, the gate having sidewalls and an interface with the gate dielectric layer;

forming nitride containing spacers over the gate sidewalls; and
after forming the spacers, exposing the substrate to oxidizing conditions effective to oxidize at least a portion of the gate interface with the gate dielectric layer.

2. The semiconductor processing method of claim 1, wherein the gate comprises a first conductive layer a portion of which defines the interface, an overlying metal, and an electrically conductive reaction barrier layer interposed between the first layer and the overlying metal.

3. The semiconductor processing method of claim 1, wherein the gate comprises polysilicon, an overlying metal, and an electrically conductive reaction barrier layer intermediate the polysilicon and the overlying metal.

1 4. The semiconductor processing method of claim 1, wherein
2 the step of forming the nitride containing spacers includes:

3 depositing a first nitride containing material over the gate;

4 depositing a second nitride containing material over the first
5 nitride containing material; and

6 anisotropically etching the first and second nitride containing
7 materials to a degree sufficient to leave the spacers over the gate
8 sidewalls.

9
10 5. The semiconductor processing method of claim 1, wherein
11 the step of forming the nitride containing spacers includes:

12 depositing a first nitride containing material over the gate;

13 anisotropically etching the first nitride containing material to a
14 degree sufficient to leave first nitride containing spacers over the gate
15 sidewalls;

16 depositing a second nitride containing material over the first
17 nitride containing spacers; and

18 anisotropically etching the second nitride containing material to a
19 degree sufficient to leave second nitride containing spacers proximate the
20 first nitride containing spacers.

6. The semiconductor processing method of claim 1, wherein the step of forming the nitride containing spacers includes:

depositing a first nitride containing material over the gate;

anisotropically etching the first nitride containing material to a degree sufficient to leave first nitride containing spacers over the gate sidewalls;

depositing a second nitride containing material over the first nitride containing spacers; and

anisotropically etching the second nitride containing material to a degree sufficient to leave second nitride containing spacers proximate the first nitride containing spacers, the step of exposing the substrate to oxidizing conditions taking place prior to depositing the second nitride containing material and after anisotropically etching the first nitride containing material.

7. The semiconductor processing method of claim 1, wherein the oxidizing conditions include an ambient temperature in the range from between about 800°C to 1050°C.

8. The semiconductor processing method of claim 1, wherein the gate includes a gate top and further comprising forming an oxidation resistant material over the gate top which, together with the nitride containing spacers, effectively encapsulates the gate.

9. The semiconductor processing method of claim 1, wherein the gate includes a gate top and further comprising forming an nitride containing oxidation resistant material over the gate top which, together with the nitride containing spacers, effectively encapsulates the gate.

10. A semiconductor processing method of forming a conductive gate comprising conducting a gate oxidation step after encapsulating the gate with oxidation resistant material.

11. The semiconductor processing method of claim 10, wherein the step of encapsulating the gate comprises forming electrically insulative sidewall spacers over the gate by:

depositing a first insulative material over the gate;

depositing a second insulative material over the first insulative material; and

anisotropically etching the first and second insulative materials to a degree sufficient to leave the insulative spacers over the gate.

12. The semiconductor processing method of claim 10, wherein the step of encapsulating the gate comprises forming electrically insulative sidewall spacers over the gate by:

depositing a first insulative material over the gate;

anisotropically etching the first insulative material to a degree sufficient to leave first insulative spacers over the gate;

depositing a second insulative material over the first insulative spacers; and

anisotropically etching the second insulative material to a degree sufficient to leave second insulative spacers over the first insulative spacers.

13. The semiconductor processing method of claim 10, wherein the gate comprises polysilicon, an overlying metal, and an electrically conductive reaction barrier layer intermediate the polysilicon and the overlying metal.

14. The semiconductor processing method of claim 10, wherein the oxidation resistant material contains a nitride material.

15. The semiconductor processing method of claim 10, wherein the gate has a gate top and the encapsulating step comprises forming a nitride containing oxidation resistant material over the gate sidewalls and gate top.

16. A semiconductor processing method of forming a conductive transistor gate over a substrate comprising the steps of:

forming a conductive gate over a gate dielectric layer on a substrate, the gate having sidewalls;

forming non-oxide spacers over the sidewalls; and

after forming the spacers, exposing the substrate to oxidizing conditions effective to oxidize at least a portion of the gate and a portion of the substrate beneath the gate.

17. The semiconductor processing method of claim 16, wherein the step of forming the non-oxide spacers comprises:

depositing a first non-oxide material over the gate;

depositing a second non-oxide material over the first non-oxide material; and

anisotropically etching the first and second non-oxide materials to a degree sufficient to leave non-oxide spacers over the gate sidewalls.

18. The semiconductor processing method of claim 16, wherein the step of forming the non-oxide spacers comprises:

depositing a first non-oxide material over the gate;

anisotropically etching the first non-oxide material to a degree sufficient to leave first spacers over the gate sidewalls;

depositing a second non-oxide material over the first spacers; and

anisotropically etching the second non-oxide material to a degree sufficient to leave second spacers over the first spacers.

19. The semiconductor processing method of claim 16, wherein the oxidizing conditions include an ambient temperature from between about 800°C to 1050°C.

20. A semiconductor processing method of forming a conductive transistor gate comprising the steps of:

forming a conductive gate stack over a gate dielectric layer on a substrate; the stack comprising polysilicon, an overlying metal, and an electrically conductive reaction barrier layer intermediate the polysilicon and the overlying metal; the gate having sidewalls and an interface with the gate dielectric layer;

forming an oxidation resistant layer over at least the gate stack sidewalls of the metal; and

after forming the oxidation resistant layer, exposing the substrate to oxidizing conditions effective to oxidize at least a portion of the gate laterally adjacent the oxidation resistant layer.

21. The semiconductor processing method of claim 20, wherein the oxidation resistant layer effectively encapsulates the gate stack.

22. The semiconductor processing method of claim 20, wherein the oxidation resistant layer comprises a nitride material.

23. The semiconductor processing method of claim 20, wherein the oxidation resistant layer comprises an oxidation resistant cap atop the overlying metal, and the step of forming the oxidation resistant layer over at least the gate stack sidewalls of the metal comprises:

- depositing a first oxidation resistant layer over the gate;
- depositing a second oxidation resistant layer over the first oxidation resistant layer; and
- anisotropically etching the first and second layers to a degree sufficient to leave sidewall spacers over at least the gate stack sidewalls between the cap and the dielectric layer.

24. The semiconductor processing method of claim 20, wherein the oxidation resistant layer further comprises an oxidation resistant cap atop the overlying metal, and the step of forming the oxidation resistant layer over at least the gate stack sidewalls of the metal comprises:

depositing a first oxidation resistant layer over the gate;

anisotropically etching the first oxidation resistant layer to a degree sufficient to leave first sidewall spacers over at least the gate stack sidewalls between the cap and the dielectric layer;

depositing a second oxidation resistant layer over the first sidewall spacers; and

anisotropically etching the second oxidation resistant layer to a degree sufficient to leave second sidewall spacers over at least most of the first sidewall spacers.

25. The semiconductor processing method of claim 20, wherein the oxidation resistant layer further comprises an oxidation resistant cap atop the overlying metal, and the step of forming the oxidation resistant layer over at least the gate stack sidewalls of the metal comprises:

depositing a first oxidation resistant layer over the gate;

anisotropically etching the first oxidation resistant layer to a degree sufficient to leave first sidewall spacers over at least the gate stack sidewalls between the cap and the dielectric layer;

depositing a second oxidation resistant layer over the first oxidation resistant layer; and

anisotropically etching the second oxidation resistant layer to a degree sufficient to leave second sidewall spacers over at least most of the first sidewall spacers, the step of exposing the substrate to oxidizing conditions taking place after anisotropically etching the first oxidation resistant layer.

26. The semiconductor processing method of claim 20, wherein the oxidizing conditions include an ambient temperature condition from between about 800°C to 1050°C.

1 27. A semiconductor processing method of forming a conductive
2 gate comprising:

3 forming a gate over a gate dielectric layer on a substrate, the
4 gate having sidewalls;

5 shielding at least a portion of the gate sidewalls with a nitride
6 containing oxidation resistant material; and

7 after the shielding, exposing the substrate to oxidation conditions
8 effective to oxidize at least a portion of the gate sidewalls laterally
9 inwardly of the oxidation resistant material, the shielding channeling
10 oxidants through the gate dielectric layer to the gate sidewalls.

11
12 28. The semiconductor processing method of claim 27, wherein
13 the shielding step comprises covering a top of the gate with the
14 oxidation resistant material.

15
16 29. The semiconductor processing method of claim 27, wherein
17 the shielding step comprises covering the gate with the oxidation
18 resistant material in at least two separate steps.

19
20 30. The semiconductor processing method of claim 27, wherein
21 the gate comprises polysilicon, an overlying metal, and an electrically
22 conductive reaction barrier layer intermediate the polysilicon and the
23 overlying metal.

31. The semiconductor processing method of claim 27, wherein the gate comprises polysilicon, an overlying metal, and an electrically conductive reaction barrier layer intermediate the polysilicon and the overlying metal, a portion of the overlying metal defining a gate top, and the shielding step further comprises forming an oxidation resistant cap atop the gate top.

32. The semiconductor processing method of claim 27, wherein the oxidizing conditions include an ambient temperature from between about 800°C to 1050°C.

33. A semiconductor processing method of forming a conductive gate comprising the steps of:

forming a patterned gate atop a substrate dielectric surface, at least a portion of the gate being conductive;

covering a top and sidewalls of the gate with oxidation resistant material; and

exposing the substrate to oxidation conditions effective to oxidize at least a portion of the gate laterally adjacent the covered sidewalls adjacent the dielectric surface.

34. The semiconductor processing method of claim 33, wherein the conductive portion of the gate comprises a reaction barrier layer and an overlying metal thereon.

35. The semiconductor processing method of claim 33, wherein the conductive portion of the gate comprises polysilicon, an overlying metal, and a reaction barrier layer interposed between the polysilicon and the overlying metal.

36. The semiconductor processing method of claim 33, wherein the covering step comprises:

depositing a first barrier material over the gate;

depositing a second barrier material over the first barrier material;

and

anisotropically etching the first and second barrier materials to a degree sufficient to leave the oxidation barriers on the gate.

37. The semiconductor processing method of claim 33, wherein the covering step comprises:

depositing a first barrier material over the gate;

depositing a second barrier material over the first barrier material;

and

anisotropically etching the first and second barrier materials to a degree sufficient to leave the oxidation barriers on the gate, the etched first barrier material defining at least one L-shaped oxidation barrier.

38. The semiconductor processing method of claim 33, wherein the covering step comprises:

depositing a first barrier material over the gate;

anisotropically etching the first barrier material to a degree sufficient to leave first oxidation barriers on the gate;

depositing a second barrier material over the first barrier material;

and

anisotropically etching the second barrier material to a degree sufficient to leave second oxidation barriers over the first oxidation barriers.

39. The semiconductor processing method of claim 33, wherein the oxidation resistant material comprises a nitride material.

40. A semiconductor processing method of forming a conductive line comprising:

forming a conductive line atop a substrate dielectric layer;
covering a top and sidewalls of the conductive line with at least one nitride material; and

oxidizing a portion of the conductive line laterally inwardly of the nitride material.

ABSTRACT OF THE DISCLOSURE

A semiconductor processing method of forming a conductive gate or gate line over a substrate includes, a) forming a conductive gate over a gate dielectric layer on a substrate, the gate having sidewalls and an interface with the gate dielectric layer; b) electrically insulating the gate sidewalls; and c) after electrically insulating the gate sidewalls, exposing the substrate to oxidizing conditions effective to oxidize at least a portion of the gate interface with the gate dielectric layer. According to one aspect of the invention, the step of exposing the substrate to oxidizing conditions is conducted after provision of a first insulating material and subsequent anisotropic etch thereof to insulate the gate sidewalls. According to another aspect of the invention, the step of exposing the substrate to oxidizing conditions is conducted after provision of first and second insulating materials and subsequent anisotropic etch thereof to insulate the gate sidewalls. According to another aspect of the invention, the step of exposing the substrate to oxidizing conditions is conducted after provision and subsequent anisotropic etch of a first insulating material, followed by provision and subsequent anisotropic etch of a second insulating material.

1 **DECLARATION OF SOLE INVENTOR FOR PATENT APPLICATION**

2 As the below named inventor, I hereby declare that:

3 My residence, post office address and citizenship are as stated
4 below next to my name.

5 I believe I am the original, first and sole inventor of the subject
6 matter which is claimed and for which a patent is sought on the
7 invention entitled: **Semiconductor Processing Methods of Forming A**
8 **Conductive Gate and Line**, the specification of which is attached hereto.

9 I hereby state that I have reviewed and understand the contents
10 of the above-identified specification, including the claims.

11 I acknowledge the duty to disclose information known to me to
12 be material to patentability as defined in Title 37, Code of Federal
13 Regulations §1.56.

14
15 **PRIOR FOREIGN APPLICATIONS:**

16 I hereby state that no applications for foreign patents or inventor's
17 certificates have been filed prior to the date of execution of this
18 declaration.

19
20 **POWER OF ATTORNEY:**

21 As a named Inventor, I hereby appoint the following attorneys and
22 agent to prosecute this application and transact all business in the
23 Patent and Trademark Office connected therewith: Richard J. St. John,
24 Reg. No. 19,363; David P. Roberts, Reg. No. 23,032; Randy A. Gregory,

Reg. No. 30,386; Mark S. Matkin, Reg. No. 32,268; James L. Price, Reg. No. 27,376; Deepak Malhotra, Reg. No. 33,560; Mark W. Hendricksen, Reg. No. 32,356; David G. Latwesen, Reg. No. 38,533; George G. Grigel, Reg. No. 31,166; Keith D. Grzelak, Reg. No. 37,144; John S. Reid, Reg. No. 36,369; Lance R. Sadler, Reg. No. 38,605; James D. Shaurette, Reg. No. 39,833; W. Bryan Farney, Reg. No. 32,651; Lia M. Pappas, Reg. No. 34,095; and Michael L. Lynch, Reg. No. 30,871.

Send correspondence to: WELLS, ST. JOHN, ROBERTS, GREGORY & MATKIN P.S., 601 W. First Avenue, Suite 1300, Spokane, WA 99204-0317. Direct telephone calls to: Lance R. Sadler (509) 624-4276.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

Variable	Mean	SD	Min	Max
Age	34.5	10.2	21	55
Gender	Male	Female		
Marital Status	Married	Single		
Education	High School	College		
Occupation	Manager	Worker		
Income	\$20,000	\$30,000		
Health Status	Good	Fair		
Stress Level	Low	High		
Life Satisfaction	High	Low		
Work-Life Balance	Good	Poor		
Family Support	Strong	Weak		
Community Involvement	Active	Passive		
Religious Beliefs	Religious	Secular		
Political Views	Conservative	Liberal		
Personal Values	Materialistic	Altruistic		
Life Goals	Short-term	Long-term		
Personal Growth	High	Low		
Self-Confidence	High	Low		
Emotional Stability	Stable	Unstable		
Resilience	High	Low		
Optimism	Optimistic	Pessimistic		
Gratitude	High	Low		
Forgiveness	High	Low		
Empathy	High	Low		
Compassion	High	Low		
Kindness	High	Low		
Generosity	High	Low		
Patience	High	Low		
Perseverance	High	Low		
Self-Discipline	High	Low		
Responsibility	High	Low		
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Honesty	High	Low		
Trustworthiness	High	Low		
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AS FILED

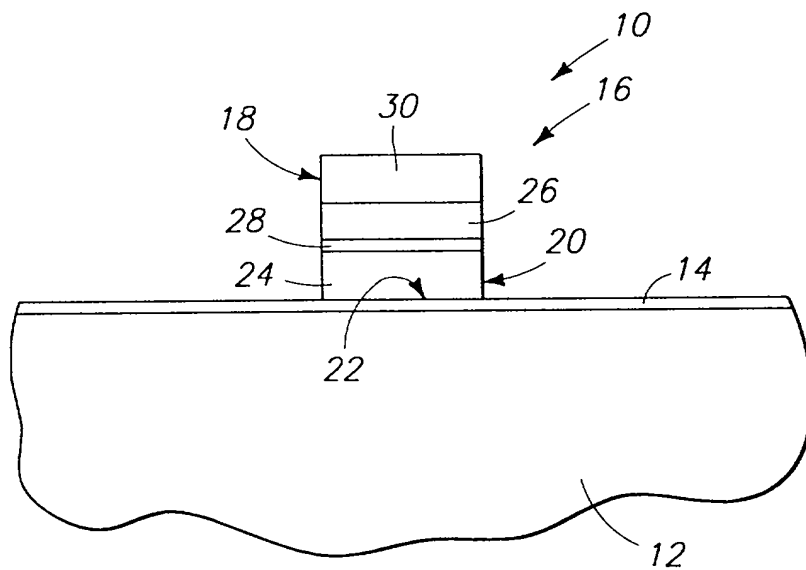


FIG. 1

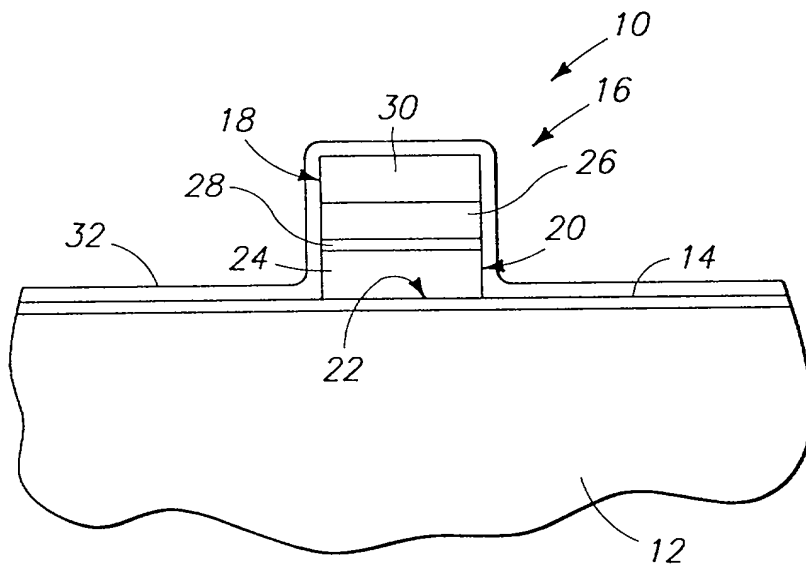


FIG. 2

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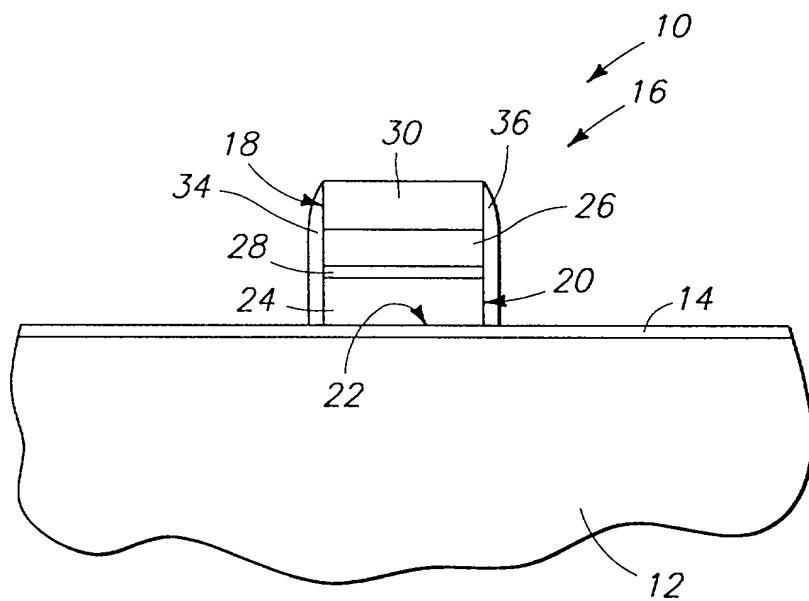


FIG. 1

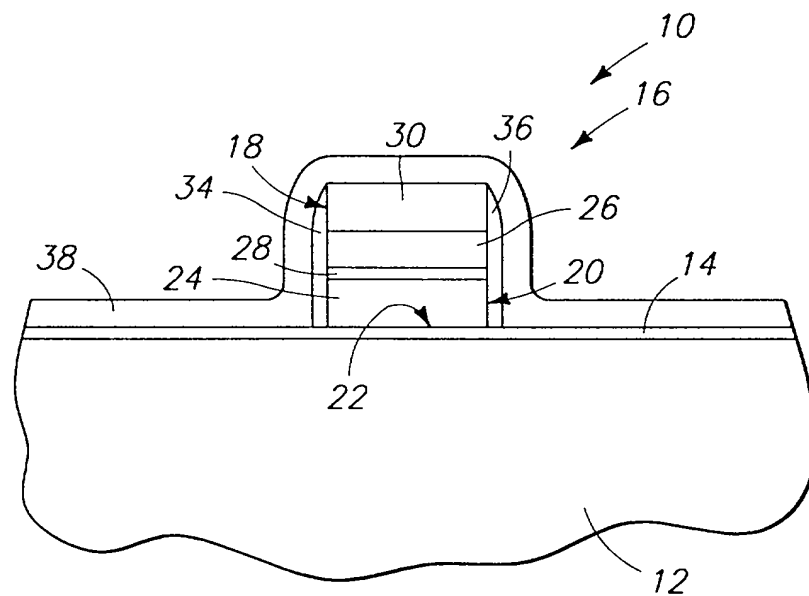


FIG. 2

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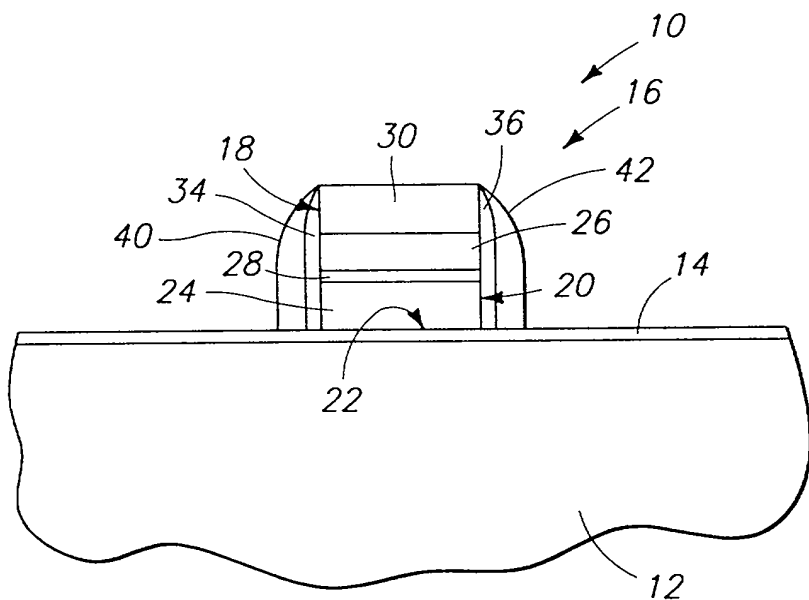


FIG. 1

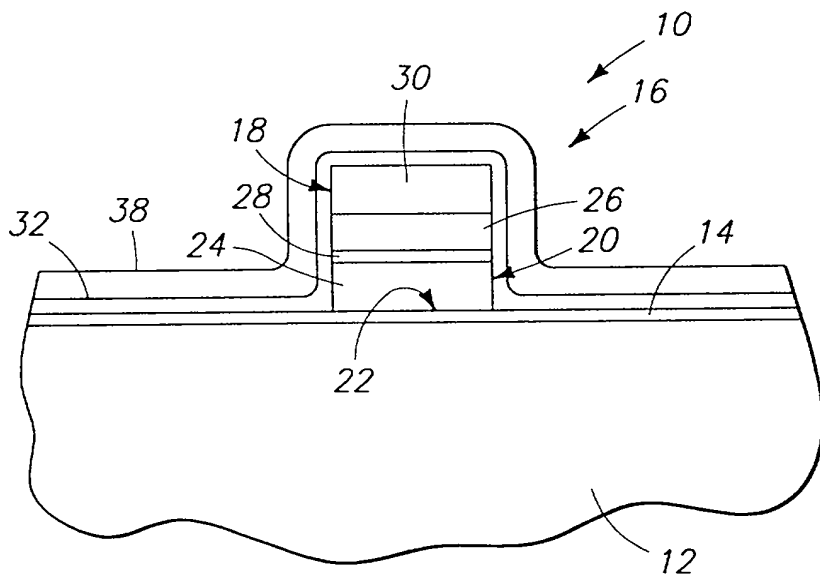
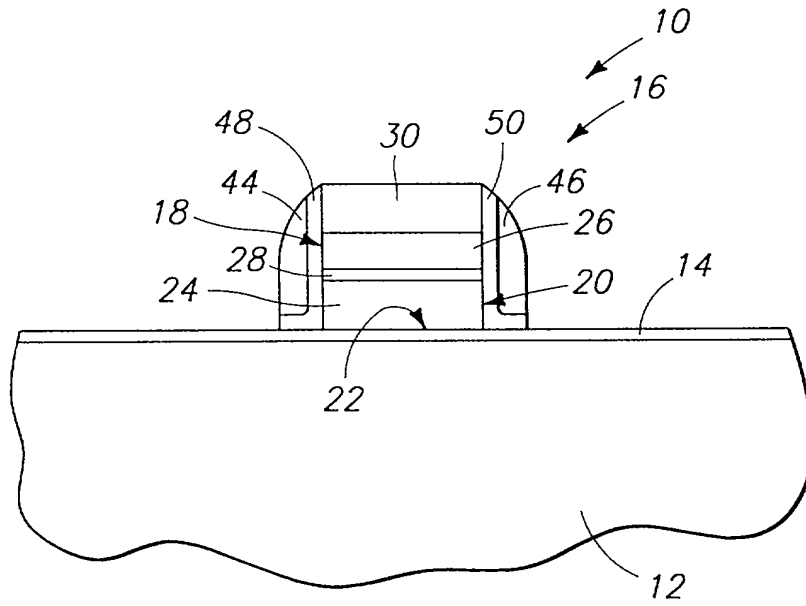


FIG. 2

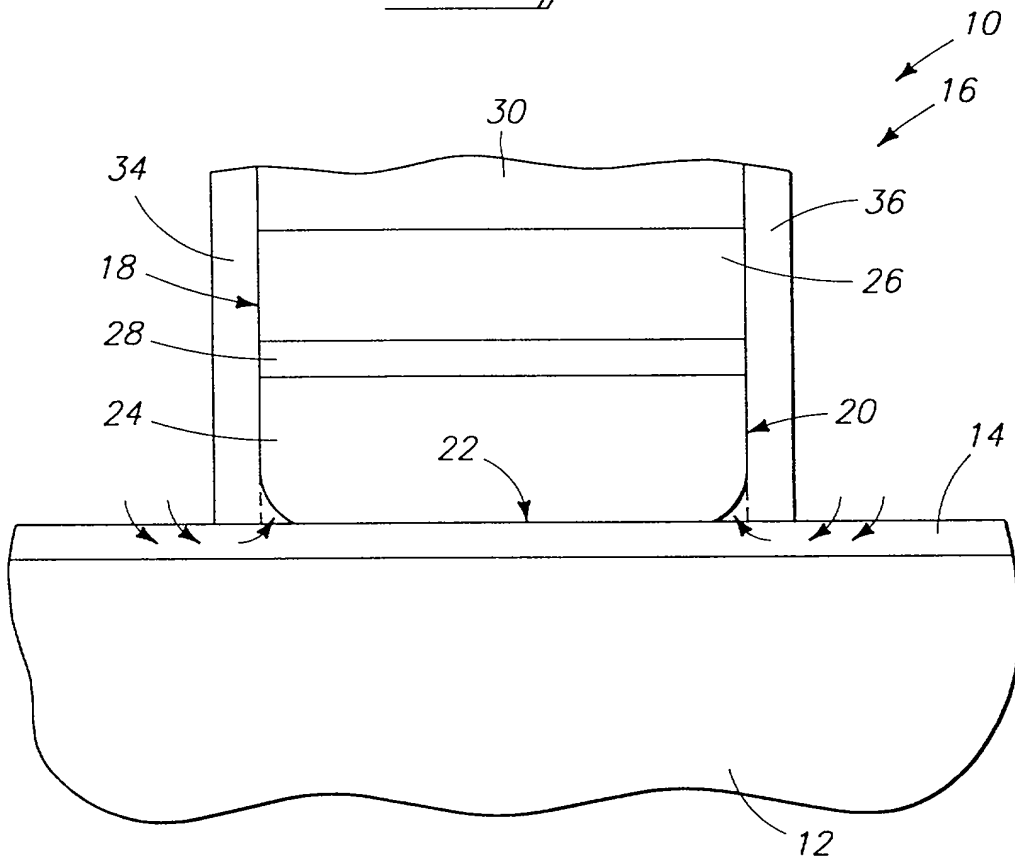
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AS FILED



II II



II II

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PRIORITY PATENT APPLICATION SERIAL NO. 08/710,353

PRIORITY FILING DATE 09/17/96

INVENTORSHIP Pai-Hung Pan

PRIORITY GROUP ART UNIT 1107

PRIORITY EXAMINER B. Mee

ATTORNEY'S DOCKET NO. MI22-898

TITLE Semiconductor Processing Methods of Forming a Conductive Gate
and Line

Assistant Commissioner for Patents

Washington, D. C. 20231

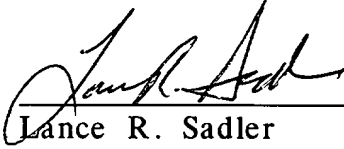
Attention: Official Draftsman

SUBSTITUTE DRAWING REQUEST

Please enter the enclosed substitute drawings in the
above-referenced application in place of drawings originally filed. The
content of the drawings are identical to those now on file in this
application.

1 Acknowledgment of receipt of the formal drawings and their
2 acceptance into the file is requested.

Respectfully submitted,

Date: 4/13/98 By: 
Lance R. Sadler
Reg. No.: 38,605
WELLS, ST. JOHN, ROBERTS,
GREGORY & MATKIN P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3817
(509) 624-4276

Enclosures: 4 Sheets of Formal Drawings, Figs. 1-8

RECEIVED 4-13-98

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 08/710,353
Priority Filing Date 09/17/96
Inventor Pai-Hung Pan
Assignee Micron Technology, Inc.
Priority Group Art Unit 1107
Priority Examiner B. Mee
Attorney's Docket No. MI22-898
Title: Semiconductor Processing Methods of Forming a Conductive Gate and Line

PRELIMINARY AMENDMENT

To: Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

From: Lance R. Sadler (Tel. 509-624-4276; Fax 509-838-3424)
Wells, St. John, Roberts, Gregory & Matkin P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3817

Sir:

Applicant preliminarily amends as follows:

AMENDMENTS

In the Specification

At p. 1 before the "Technical Field" section, please insert the following:

--RELATED PATENT DATA

This patent resulted from a continuation application of U.S. Patent Application Serial No. 08/710,353, filed September 17, 1996, entitled "Semiconductor Processing Methods of Forming a Conductive Gate and

Line", naming Pai-Hung Pan as inventor, and which is now U.S. Patent No. 5,739,066, the disclosure of which is incorporated by reference--.

In the Claims

Cancel claims 1-40 without prejudice.

Please add claims 41-52 as follows:

41. A semiconductor processing method of forming a conductive transistor gate over a substrate comprising the steps of:

forming a conductive gate over a gate dielectric layer on a substrate, the gate having sidewalls and an interface with the gate dielectric layer;

forming sidewall spacers over the gate's sidewalls, the sidewall spacers joining with the gate dielectric layer; and

after forming the sidewall spacers, exposing the substrate to oxidizing conditions effective to channel oxidants through the gate dielectric layer and underneath the sidewall spacers joined therewith to oxidize at least a portion of the gate interface with the gate dielectric layer.

42. The method of claim 41, wherein the sidewall spacers comprise nitride.

1 43. The method of claim 41, wherein the gate comprises a first
2 conductive layer a portion of which defines the interface, an overlying
3 metal, and an electrically conductive reaction barrier layer interposed
4 between the first layer and the overlying layer.

5
6 44. The method of claim 41, wherein the forming of the sidewall
7 spacers includes:

8 depositing a first material over the gate;

9 depositing a second material over the first material;

10 anisotropically etching the first and second materials to a degree
11 sufficient to leave the spacers over the gate's sidewalls, the spacers
12 being defined by both the first and second material.

13
14 45. A semiconductor processing method of forming a conductive
15 gate comprising:

16 forming sidewall spacers over a conductive gate's sidewalls
17 sufficiently to cover all conductive material comprising said sidewalls; and

18 after forming the sidewall spacers, conducting an oxidizing step by
19 channeling oxidants through a layer which underlies the gate and the
20 sidewall spacers, and which is outwardly exposed laterally proximate the
21 sidewall spacers.

22
23 46. The method of claim 45, wherein said layer through which
24 oxidants are channeled comprises a gate dielectric layer.

1 47. The method of claim 45, wherein the gate comprises
2 polysilicon, an overlying metal, and an electrically conductive reaction
3 barrier layer intermediate the polysilicon and the overlying metal.

4
5 48. The method of claim 45, wherein the forming of the sidewall
6 spacers comprises:

7 depositing a first material over the gate;
8 depositing a second material over the first material; and
9 anisotropically etching the first and second materials to a degree
10 sufficient to leave the sidewall spacers over the gate's sidewalls.

11
12 49. The method of claim 45, wherein the forming of the sidewall
13 spacers comprises:

14 depositing a first material over the gate;
15 anisotropically etching the first material to a degree sufficient to
16 leave first sidewall spacers over the gate;
17 depositing a second material over the first sidewall spacers; and
18 anisotropically etching the second material to a degree sufficient
19 to leave second sidewall spacers over the first sidewall spacers.

1 50. A semiconductor processing method of forming a conductive
2 transistor gate over a substrate comprising the steps of:

3 forming a conductive gate over a gate dielectric layer on a
4 substrate, the gate having sidewalls disposed over the dielectric layer, the
5 dielectric layer extending laterally outward of the sidewalls;

6 forming non-oxide material over the gate and dielectric layer;

7 anisotropically etching the non-oxide material to form non-oxide
8 spacers over the sidewalls, the spacers joining with the gate dielectric
9 layer; and

10 after anisotropically etching the non-oxide material to form the
11 spacers, exposing the substrate to oxidizing conditions effective to oxidize
12 at least a portion of the gate.

13
14 51. The method of claim 50, wherein the forming of the non-
15 oxide material and the anisotropically etching thereof comprises:

16 depositing a first non-oxide material over the gate;

17 anisotropically etching the first non-oxide material to a degree
18 sufficient to leave first spacers over the gate sidewalls;

19 depositing a second non-oxide material over the first spacers; and

20 anisotropically etching the second non-oxide material to a degree
21 sufficient to leave second spacers over the first spacers.

1 52. A semiconductor processing method of forming a conductive
2 gate comprising the steps of:

3 forming a patterned gate atop a substrate dielectric surface, at
4 least a portion of the gate being conductive, the conductive portion
5 comprising:

6 a polysilicon layer,

7 an overlying metal, and

8 a reaction barrier layer interposed between the polysilicon
9 and the overlying metal;

10 covering a top and sidewalls of the gate with oxidation resistant
11 material, said covering comprising:

12 depositing a first barrier material over the gate,

13 depositing a second barrier material over the first barrier
14 material, and

15 anisotropically etching the first and second barrier materials
16 to a degree sufficient to leave the oxidation barriers on the gate; and

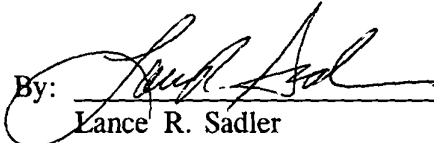
17 exposing the substrate to oxidation conditions effective to oxidize
18 at least a portion of the gate laterally adjacent the covered sidewalls
19 adjacent the dielectric surface.
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REMARKS

This application is a continuation application of U.S. Patent Application Serial No. 08/710,353. Claims 1-40 have been canceled without prejudice. Claims 41-52 have been added and are believed to be in condition for allowance. Accordingly, Applicant respectfully requests a Notice of Allowability be issued forthwith.

Respectfully submitted,

Dated: 4/13/98

By: 
Lance R. Sadler
Reg. No. 38,605